SUMMER PROJECT REPORT
IMPLEMENTING DELAYS IN THE SEQUENCER

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ABSTRACT

The Sequencer is the source of the control signals for the Analog Front End, (AFE). In order to synchronize signals from the fiber detectors at the Forward Proton Detector (FPD) with the rest of the DØ detector, it is necessary to delay the Sequencer Controller signals (due to the time of flight and cable delays of the forward Proton Detector).

Contents:

1. INTRODUCTION

The Forward Proton Detector, FPD, is a series of scintillation fiber detectors. These scintillation fiber detectors are housed in set of 18 Roman Pots and are readout by multi-anode photomultiplier tubes. The Roman Pots are positioned on both sides of the DØ detector (proton and anti-proton side) allowing the observation and measurement of scattered protons and anti-protons. This allows access to a wide range of soft and hard diffractive physics.

The FPD detectors are located upstream and downstream of the Central DØ detector see Figure 1. This introduces a problem when the FPD group data has to be integrated into the system because of different cable runs and the time of flight of the particles. For the FPD group to observe the same events, and also to integrate their data in the system, delays in they data acquisition are necessary. It is proposed to create delays in the FPD electronics. As described later in this document, there are three different delays that the FPD has to provide. The main focus of this document is the creation of two of these delays. The third delay is proposed to be created in the Analog Front End, AFE. Further discussion on this third delay is provided in the conclusion.

2. THEORY

I. Delay Times

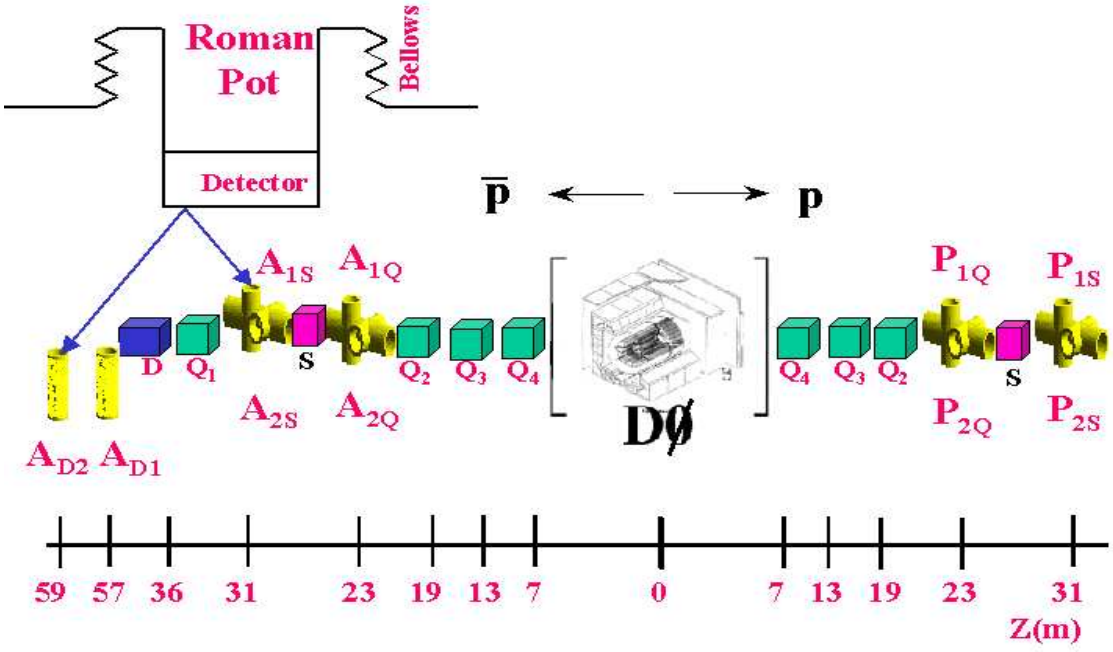

Figure 1. Layout of the Forward Proton Detector.

Delays are necessary for the FPD because of its position from the collision hall. The theoretical delays were calculated by using the following equation

$$T_d = T_{of} + T_{cd} \quad (1)$$

where T_d is the total delay

T_{of} is time of flight of particles.

T_{cd} is cable delay.

Since the particle are traveling at approximately the speed of light, *TOF* calculated by the following equation.

$$T_{of} = \frac{d}{c} \quad (2)$$

where d is the distance from point of collision

c is the speed of light.

The speed of signals through the cables used to connect the electronic is 0.75c. From the equations (1), (2) and the speed of signals in cables the total delays were calculated for each pot location and shown in Table 1.

Table 1. Shows theoretical delay times

POTS	DISTANCE	T_{of}	T_{cd}	T_d
P1	23m	77 ns	244 ns	321 ns
A1	23m	77 ns	244 ns	321 ns
P2	31m	103 ns	472 ns	575 ns
A2	31m	103 ns	472 ns	575ns
*D1	57m	190 ns	446 ns	636 ns
*D2	59m	197 ns	446ns	636 ns

Neglecting the small difference in the distance D1 and D2, Table 1 shows that there are three different delays.

II. FPD Electronics

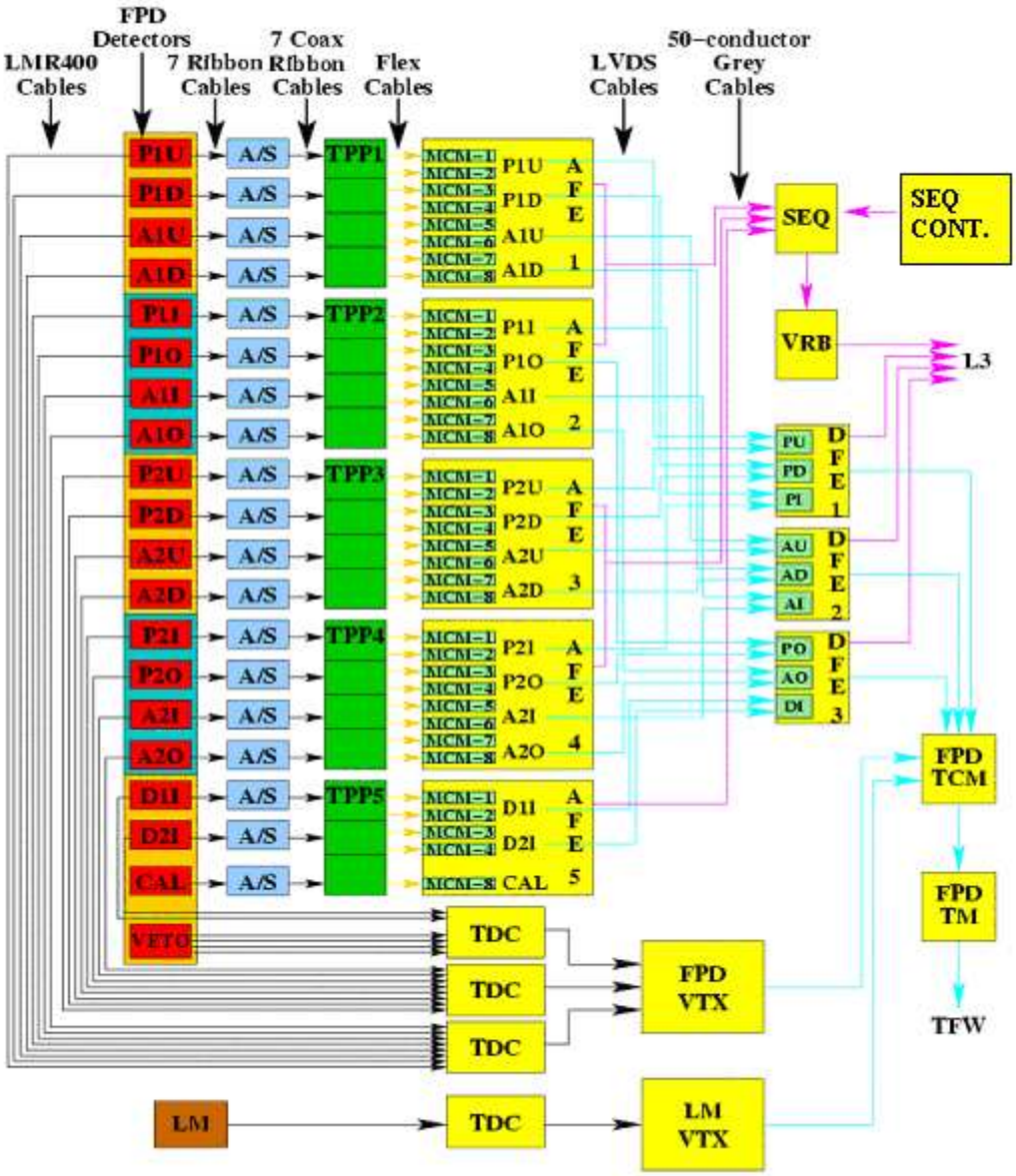

Figure 2. Shows a block diagram of the FPD electronics with the different types of cable runs.

For this projects the important players are the Sequencer Controller, SVX Sequencer which is commonly called the Sequencer and the Analog Front End, AFE. Basically the Sequencer Controller sends the information needed for the Sequencer to generate the control signal for the AFE. The AFE is the interface for the SVX chips (Silicon Vertex) as seen in figure 2.

i. Sequencer Controller

In slot 1 of the Sequencer crate resides the Sequencer Controller [1]. It takes the Serial Command Link (SCL) signals and transforms it into pairs of Sequencer control signals (NRZ & Clock). Each sequencer receives its own pair of signals with adjusted timing. These signals provides information for the Sequencer to produce the proper times to reset the preamps, trigger, digitize, and read out data. NRZ stands for Non-Return to Zero and is a basic data transmission protocol. The Clock line acts as a strobe for NRZ. NRZ is made up of a continuous stream of seven-bit packets, which is synchronized with the accelerator, each bit being the same duration as one Tevatron RF cycle. The bits in each packet consist of one framing bit which is always high, a bit which is high if a beam crossing is imminent, four bits representing the command desired, and one parity bit (odd parity), as seen in Figure 3. If the controller detects that a framing bit is zero, a NoSynch indication will occur, readable via 1553 or front panel LED. Synch is automatically re-established by sending only the framing bit for three cycles. This also happens to be the Idle command. The four command bits are defined in Table 2.

FRAME	CROSSING	DATA	DATA	DATA	DATA	PARITY
1	2	3	4	5	6	7

Figure 3. Seven bit packet of the NRZ Signal

Table 2. Command codes encoded in NRZ

COMMANDS	Four Bit Code
Idle	0 0 0 0
Acquire	0 0 0 1
Trigger	0 0 1 1
Ramp	1 0 1 0
Digitize	0 0 1 0
Readout	0 1 1 0
Reset_Preamp	0 1 0 1
Cal_Inject	0 1 1 1
Extract Pipeline Charge	1 0 1 1
Reserved_9	1 0 0 1
Reserved_4	0 1 0 0
Reserved_C	1 1 0 0
Reserved_8	1 0 0 0
Reserved_F	1 1 1 1
Reserved_D	1 1 0 1
Reserved_E	1 1 1 0

ii. Sequencer

Residing in slots 2 through 21 of each of eight Eurocard crates in the D0 Detector Platform is the SVX Sequencer boards are 9U by 280mm circuit boards that [2]. Its basic purpose is to control the SVX chips for data acquisition and when a trigger occurs, to gather the SVX data and relay the data to the VRB boards in the Movable Counting House. Functions and features are as follows:

- Initialization of eight SVX chip strings using the MIL-STD-1553 data bus.
- Real time manipulation of the SVX control lines to effect data acquisition, digitization, and readout based on the NRZ/Clock signals from the VRB Controller.
- Conversion of 8-bit electrical SVX readout data to an optical signal operating at 1.062 Gbit/sec, sent to the VRB. Eight HDIs will be serviced per board.
- Built-in logic analyzer which can record the most important control and data lines during a data acquisition cycle and put this recorded information onto the 1553 bus.
- Identification header and end of data trailer tacked onto data stream.
- 1553 register which can read the current values of the control and data lines.

- 1553 register which can test the optical link.
- 1553 registers for independent phasing of the SVX DVALID signals, crossing pulse width, calibration pulse voltage, and calibration pipeline select.
- 1553 register for reading the optical drivers' status link.
- Abundant front panel displays and LEDs show the board status at a glance.
- In-system programmable EPLDs are programmed via 1553 or Altera's "Bitblaster" [5].

iii. Analog Front End

The Analog Front End boards for the Forward Proton Detector - FPD_AFE, are the same AFE boards for the Central Fiber Tracker, Forward Preshower and Central Preshower sub-detectors of the DØ detector. The FPD_AFE boards have the following functions [3]:

- To process the signals from the Forward Proton Detector MAPMT's, to condition and discriminate signals from these devices within the Multi Chip Module - MCM,
- To send out hit pulses to the FPD_DFE boards, that will generate Level 1 Trigger signals.
- To send out to L3 DAQ analog signals converted by SVX II chips, in the standard event data block, and other L1 trigger monitoring information. To get D0 clock and trigger signals from the Serial Command Link.

The 8-MCM AFE contains a number of subsystems [4].
The essential subsystems are as follows:

- Interface to MIL-STD 1553
- Dual-port RAM between 1553 interface and internal microprocessor
- Microprocessor with built-in A/D converter
- DAC system to develop all control voltages for SIFT chips in the MCMs
- A clock generation system to develop all required timing clocks for the SIFT chips
- Eight Multi-Chip Modules (MCMs) that perform measurement of the analog signals
- A 'Virtual SVX' (VSVX) system to buffer discriminator data for readout with SVX data
- An interface to the SVX Sequencer for SVX control and readout
- Analog monitoring for the cassette temperature and VLPC bias control
- High speed data multiplexing system which takes all discriminator data from the SIFT chips and sends it via LVDS links to the Digital Boards.

The heart of the AFE is eight Multi-Chip Modules (MCMs) which each contain four

SIFT discriminator chips and one SVX II charge-sensitive ADC. Each MCM can 'see' up to 72 channels of charge input. Every 132ns the SIFTs provide one bit of discriminator output per channel, where a '1' indicates that the charge delivered to the SIFT was above a threshold set by a control voltage. The charge collected by each channel of each SIFT is transferred using a switched-capacitor charge pump to an SVX II chip such that the entire event is stored in the analog pipeline of the SVX. Should the discriminator pattern of this and all other trigger AFE boards indicate an interesting event, the Level 1 Trigger initiates a readout of the SVX II chips in all the AFEs, which provide 8-bit digitization of the stored charges, providing analog readout of the same charge pattern that caused the trigger in the first place.

3. Methods of Implementing the Delays

The following methods to create the delays were discussed :

- Delaying the Control Signals of the AFE
- Delaying the NRZ signal on the Sequencer
- Delaying the NRZ signal going to the sequencer from the Sequencer Controller

I. Delaying the Control Signals of the Analog Front End

Delaying the Control Signals of the Analog Front End (AFE), involves delaying the control signals coming from the Sequencer, going to the AFE. Delaying these control lines will in essence create an overall delay in the sequence of events within the Analog Front End.

II. Delaying the NRZ signal on the Sequencer

Delaying the NRZ signal on the Sequencer involves delaying the NRZ on the Sequencer. In design the Sequencer board, Mike Utes created space and wiring connection to introduce a spare PLD. By re-routing the NRZ signal through a PLD that was designed to create delays in an inputted signal, a delayed NRZ signal can be produced. This delayed NRZ can routed to the other PLD's that creates the control signal for the AFE. Thus creating a delayed control signals. This document is describes the implementation of this method.

III. Delaying the NRZ signal going to the sequencer from the Sequencer Controller

Delaying the NRZ signal going to the sequencer from the Sequencer Controller involves delaying the generation of the NRZ signal. In the designing the Sequencer, Mike Utes, provided the capability of programming delays in the generation of the NRZ signal in sequencer controller. Thus it is possible to program in the appropriate delays.

VI. Advantages and Disadvantage of each method

The comparison between the different methods of delays is seen in Table 3.

Table 3. The comparison between the different types delay methods.

Delaying Control lines	Delay in Sequencer	Delay in Sequencer Controller
No Hard-ware modification but an addition board is need	Hard-ware modification needed	No Hardware modification needed
No extra rack space	No extra rack space	Needs its own crate
Delays cannot be changed remotely	Delays can be remotely change	Delays can be change remotely.
Code need to written for FPGA	Code need to written for PLD	No new code
Many signal have to be delayed	Two signals have to be delayed	Two signals have to be delayed

Due to the complexity of the solution , the cost and space limitations of the third solution, we have chosen to implement the second solution, delaying the Sequencer controller.

4. Sequencer Delay Design

I. Overview of design

The Sequencer presently has three Programmable Logic Devices, PLD, as seen in Figure 1. The first PLD takes the serial NRZ signal on the MIL-STD 1553 twisted pair cable, from the sequencer and checks parity and synchronization. It then decodes the NRZ serial and produces another NRZ signal containing commands for the different control signal for the Analog Front End as seen in Figure 4. The Sequencer Delay design is basically the delaying of this decoded NRZ signal. These delays are created in the New PLD, placed on the board, as seen in Figure 5. From Figure 5 it can be seen that two different delays are possible.

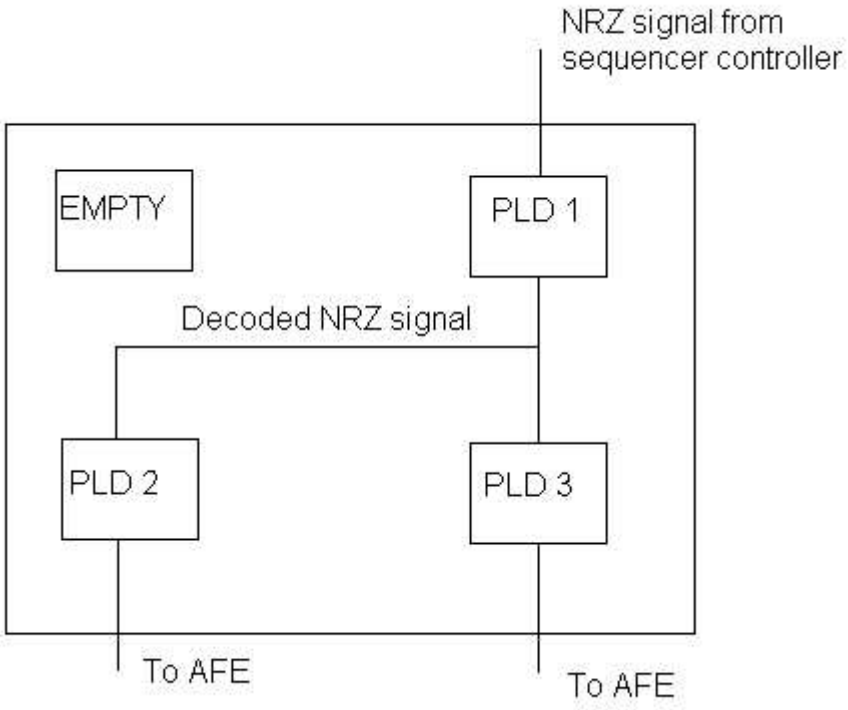

Figure 4. Simple block diagram of Sequencer before modification.

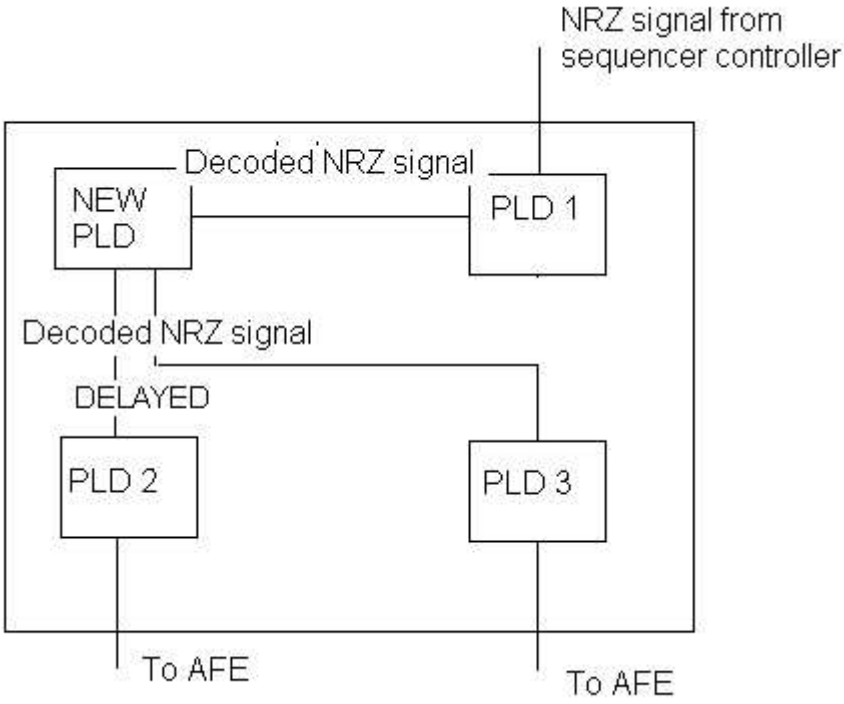

Figure 5. Simple block diagram of Sequencer After modification

The NEW PLD contains two separate programmable delay blocks as seen in Figure 6. DELAY BLOCK 1 offers a fix delay of 81ns. While DELAY

BLOCK 2 and DELAY BLOCK 3 are programmable delay blocks ranging from 0 to 301ns and 254ns to 555ns respectively. This allows delays ranging 81ns to 382ns and delays ranging from 335ns to 636ns. The delay register contains the data word that sets the required delays.

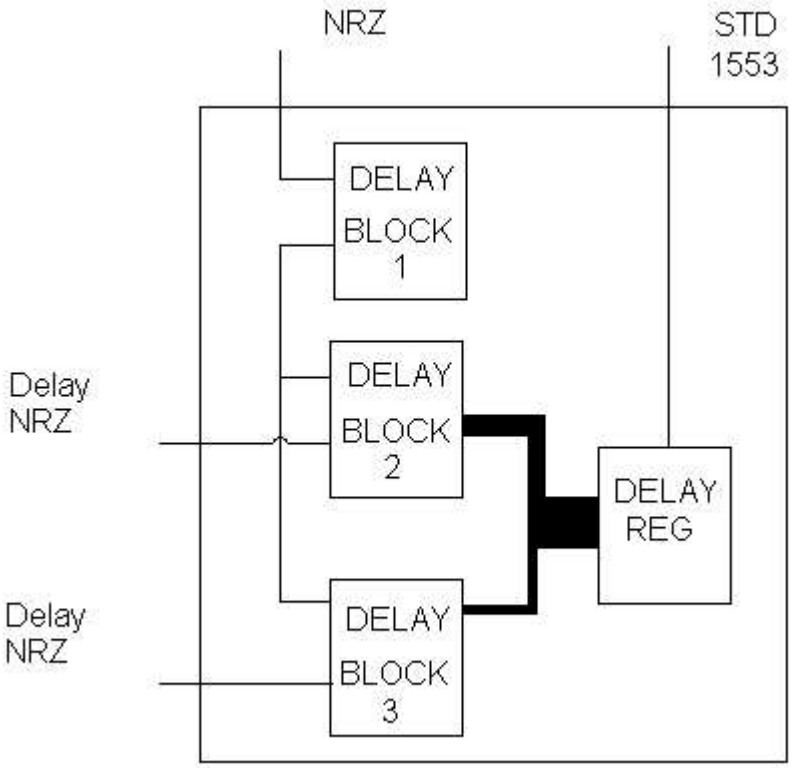

Figure 6. Block Diagram of the NEW PLD

II. Design of Version 1

Figure 7 shows the top level design for the New PLD. It contains all the blocks mention above. Figure 8 shows the hierarchy of the design produced by Altera. Table 4 gives the summary of pin usage and the overall utilization of the device. Pin layout and resource usage is seen in the Appendix.

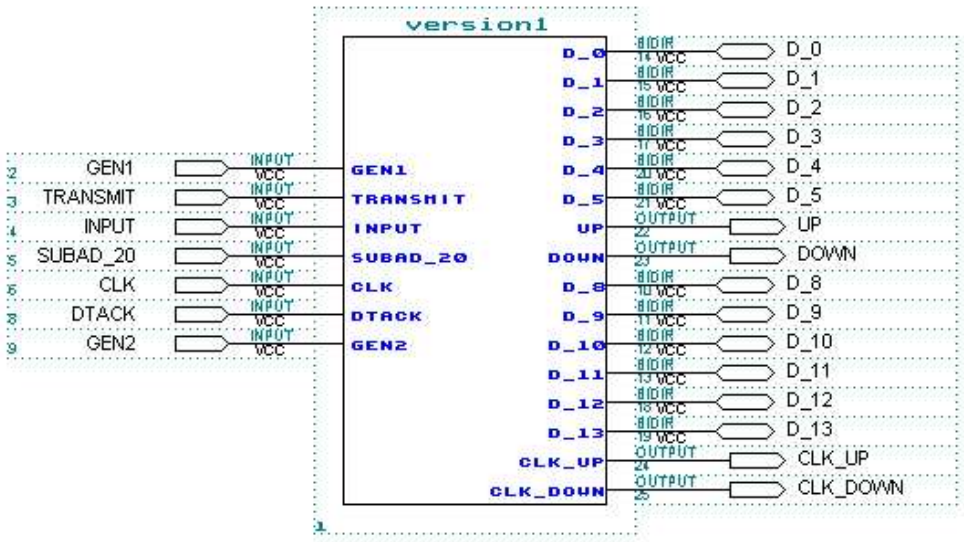

Figure 7. Top level of project design version 1.

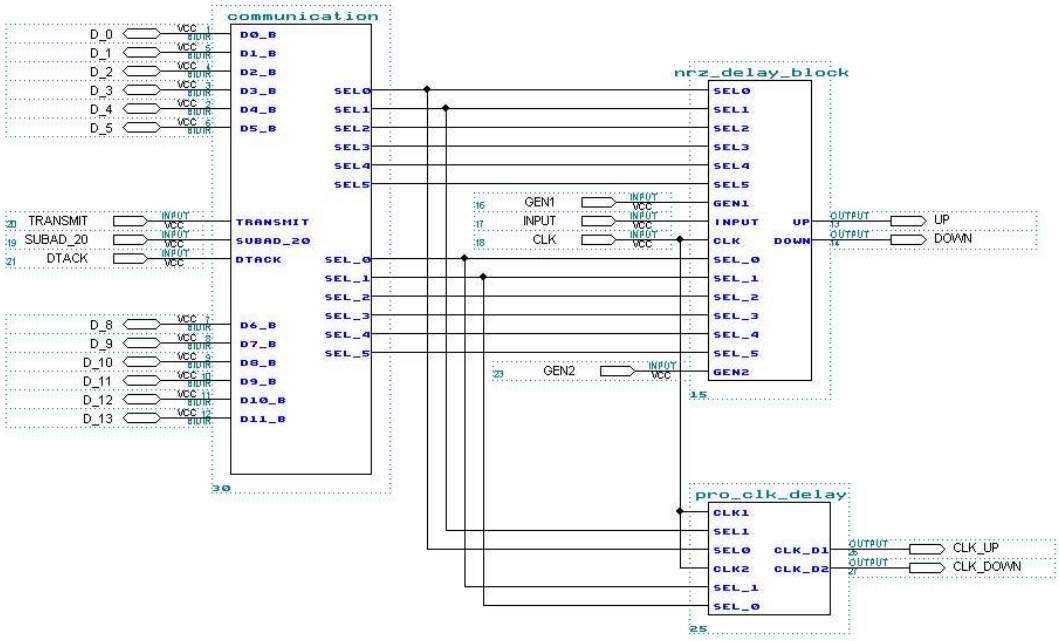

Figure 8. Hierarchy of project design version 1.

Table 4. Summary of Project

Chip/ POF	Device	Input Pins	Output Pins	Bidir Pins	LCs	Shareable Expanders	% Utilized
version1	EPM7128EQC100-7	7	4	12	73	0	57 %
User Pins:		7	4	12			

Schematic of version1

The schematic of version 1 is seen in Figure 9. The schematic can be divided into three blocks. These block are :

- The Communication
- The NRZ delay block
- The clock delay block

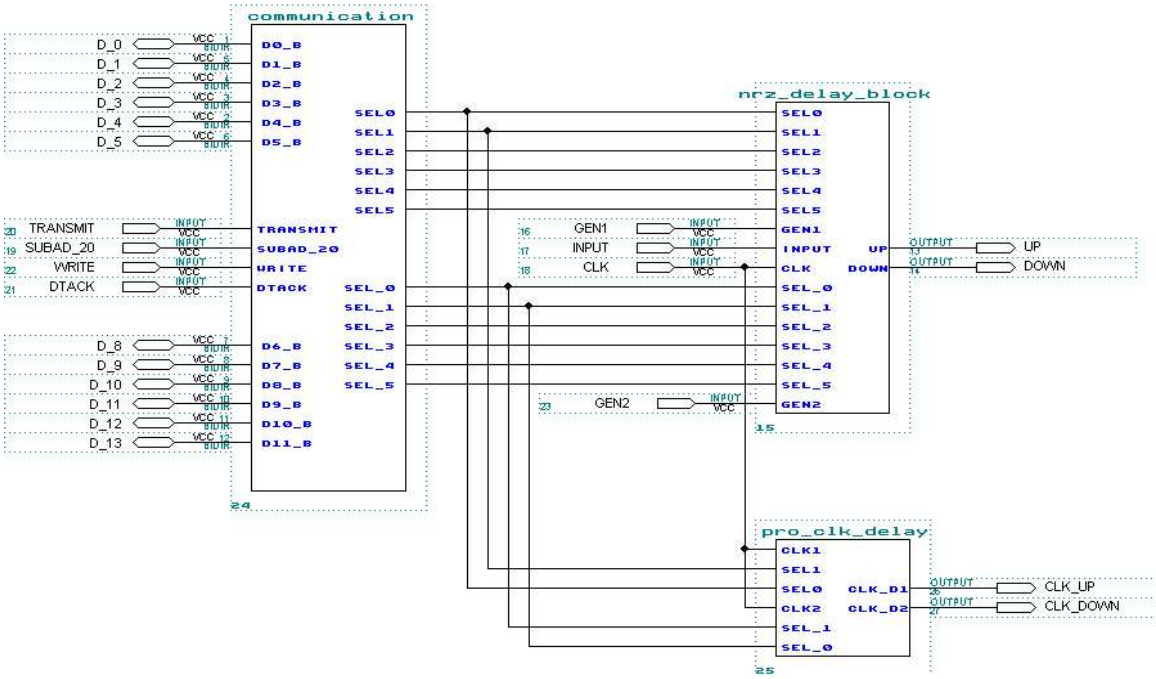

Figure 9. Schematic of version1.

III. Design of Communication block

The communication block consists of a 12 bit register which holds the 12 bit word used to program in the delay. This 12 bit register samples the data bus when SUBAD_20 goes low and Transmit goes low and DTACK goes high, storing the data on the bus in the 12 bit register.. When transmit goes high and SUBAD_20 goes low, this allows the data word in the 12 bit register to be read by the data bus. Schematic for the communication block is seen in Figure 10 and the schematic for the 12 bit register is seen in Figure 11 .

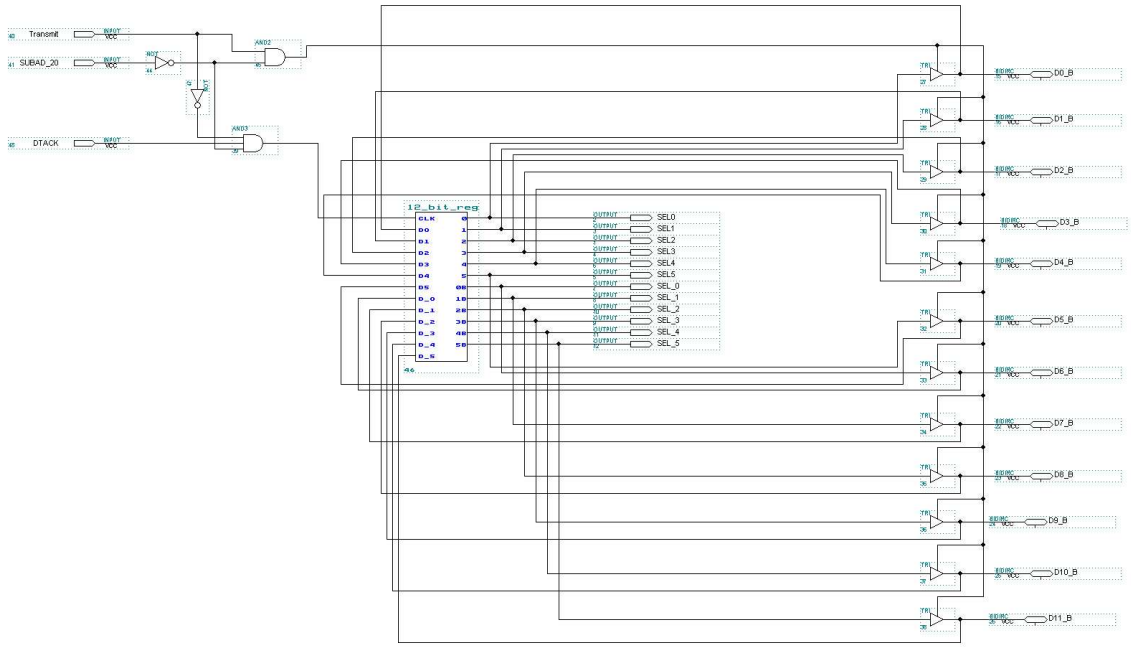

Figure 10. Schematic for Communication Block.

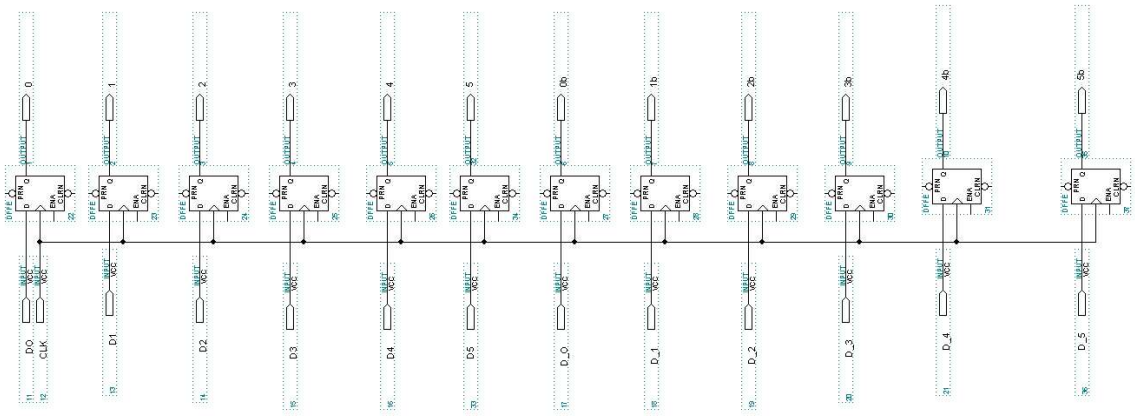

Figure 11. Schematic for 12 bit register.

VI. Design of NRZ delay block

As shown in Figure 12 the NRZ block is made up of the three blocks described earlier in the Report, i.e. Block1, Block2, Block3.

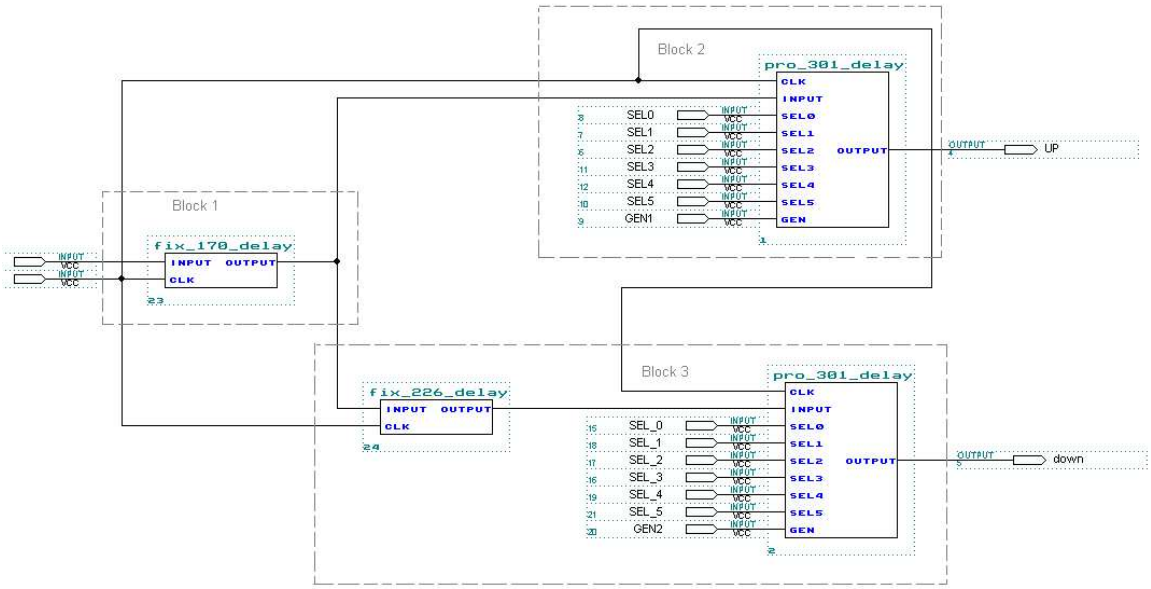

Figure 12 . Schematic of the NRZ delay Block.

i. DELAY BLOCK 1

Delay Block 1 is a fixed delay block, which consists of a daisy chain of D, flip-flops to produce 170ns delay as seen in Figure 13. This fix delay block feeds two programmable delay blocks DELAY BLOCK 2 and DELAY BLOCK 3.

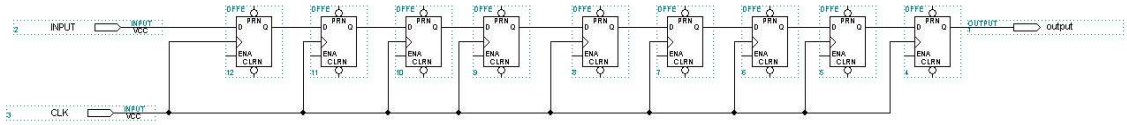

Figure 13. Schematic for DELAY BLOCK 1(170ns delay block).

ii. DELAY BLOCK 2

Delay Block 2 consists of a programmable 283 ns delay block and a programmable 18ns delay block as seen in Figure 14. These two blocks together creates a programmable 301ns delay block.

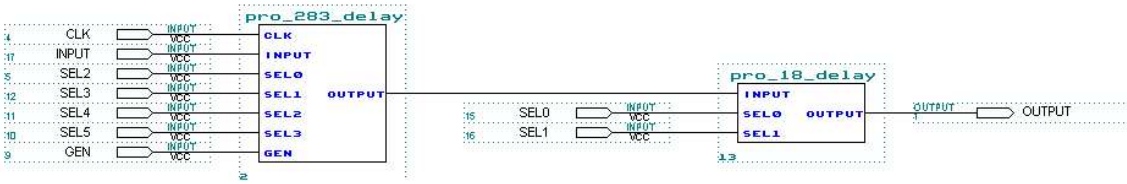

Figure 14. Schematic of DELAY BLOCK 2 delay (programmable 301ns delay).

The programmable 283ns delay block consisted of daisy chain of 15 D flip-flop where the output of each flip-flop is connected to a specific input of a 16-1 multiplexer.

Figure 15 shows the schematic of the programmable 283ns delay block. Figure 16 shows the schematic of the 16-1 multiplexer.

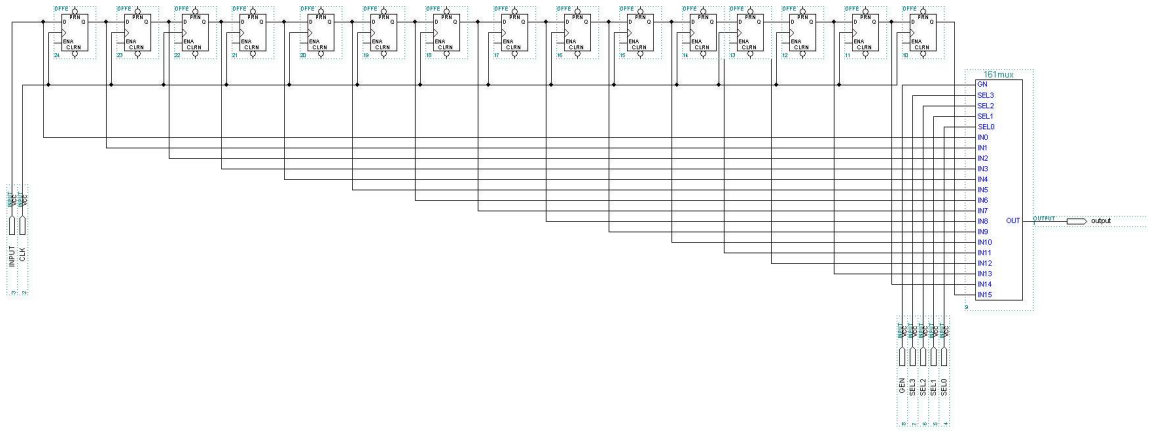

Figure 15. Schematic of programmable 283ns delay.

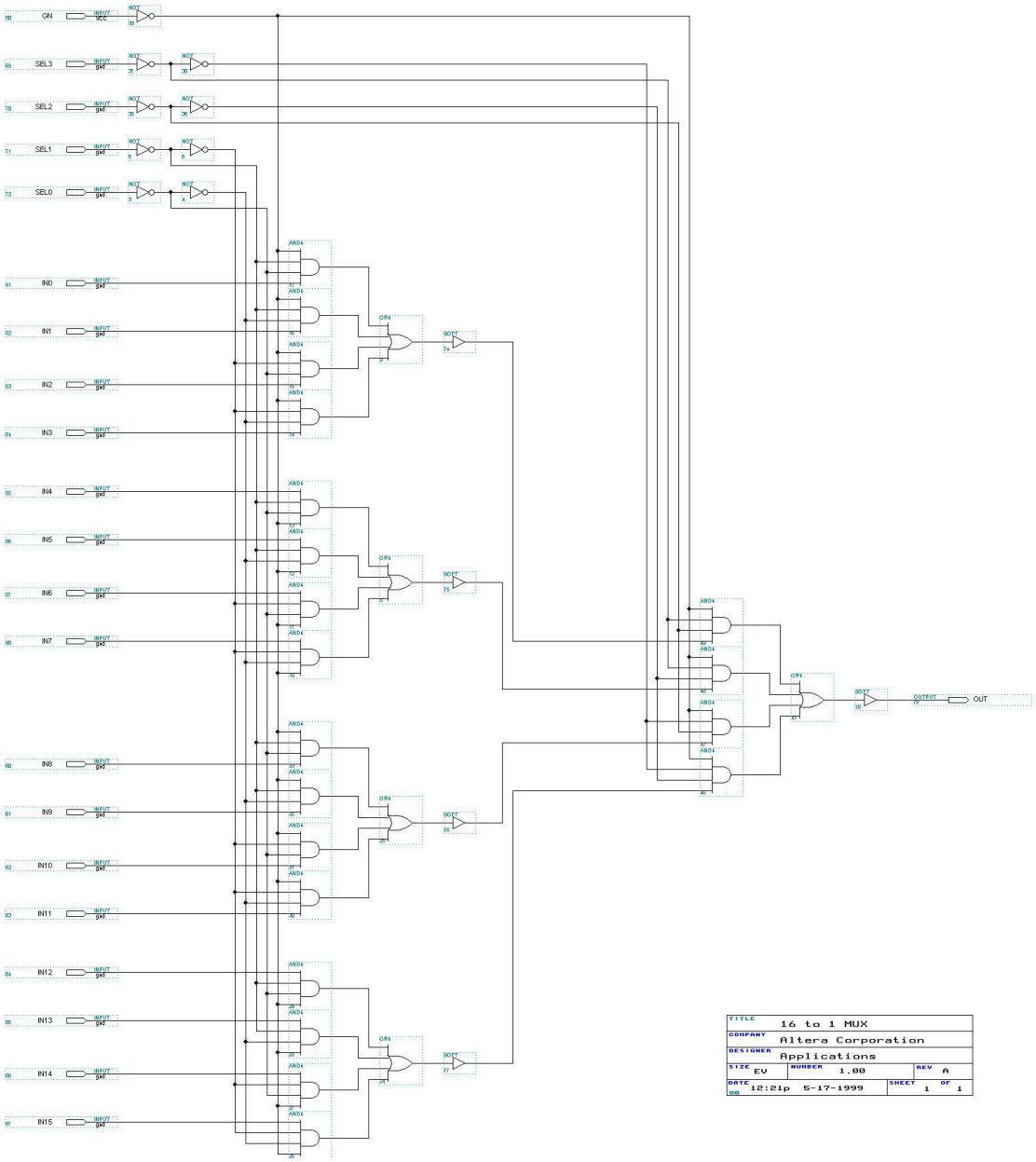

Figure 16. Schematic of 16-1 multiplexer.

The programmable 18ns delay block consisted of daisy chain of 4 logic cells where the output of each logic is connected to a specific input of a 4-1 multiplexer. Figure17 shows the schematic of the programmable 18ns delay block. Figure 18 shows the schematic of the 4-1 multiplexer.

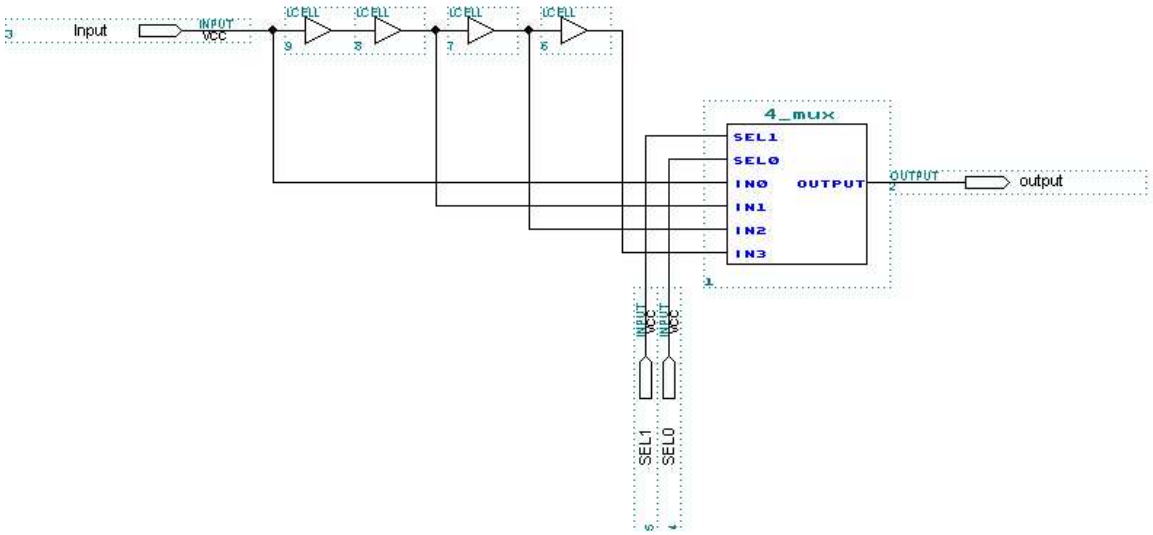

Figure 17. Schematic of programmable 18ns delay.

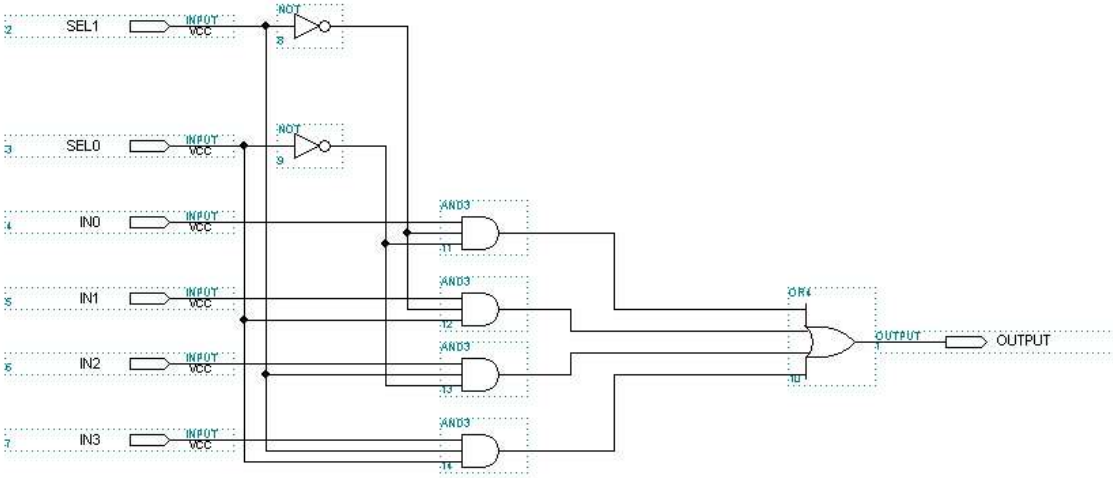

Figure 18. Schematic of 4-1 multiplexer.

iii. DELAY BLOCK 3

DELAY BLOCK 3 consisted of a fixed 254ns delay block, which consisted of a daisy chain of 15 D flip-flops and a programmable 301ns delay block as seen in Figure 19. The schematic for the fixed 226ns delay block is seen in Figure 20.

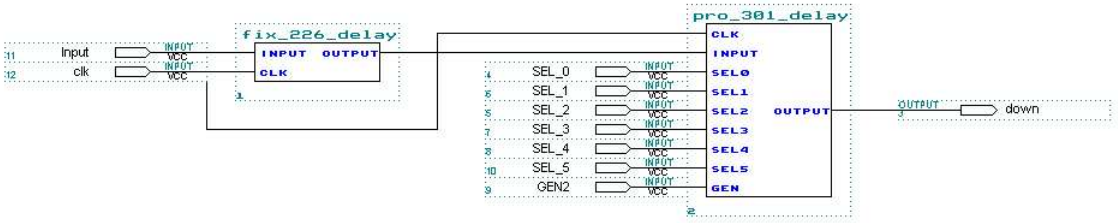

Figure 19 . Schematic for BLOCK 3.

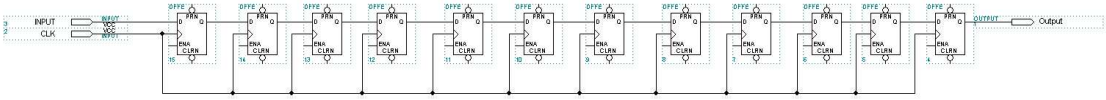

Figure 20 . Schematic for 226ns delay block

V. Design of Programmable clock delay

The Programmable Clock Delay, delays the clocks for the Upper and Lower PLD. This is in order to keep the phrase relation of the delayed NRZ with that of the clock signal to the PLD's. The programmable clock delay consists of two separate programmable 18ns delay blocks. The select lines of this block are connected to the same select lines of the programmable 18ns delay block in the NRZ delay block. The programmable 18ns delay block is the similar to the one describe earlier.

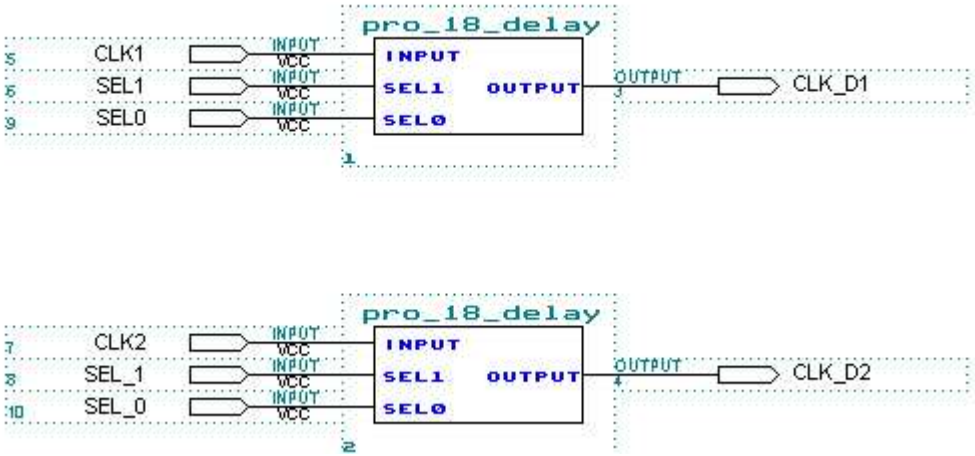

Figure 21. Schematic of programmable clock delay

5. Simulation Results

Table 5 and Table 6 shows the simulated results for the possible delays that version 1 can provide. Figures 22 and 23 shows the simulated results for the minimum and maximum delays possible, it also shows the clock relations for the delays. From the simulated results the minimum and maximum for the upper and lower are as follows.

Table 5. Shows the Min and Max of Upper and Lower PLD delay

	Upper PLD	Lower PLD
min	188.8 ns	414.4 ns
max	494.8ns	720.4 ns

Range of delays = 306 ns
Resolution approximately 5ns
The delayed clock is off-center from the center of the input signal by approximately 3ns.

Note selection of delays are non-linear and the results are simulated result with an error +/- 3ns. Graph for possible delays is seen in the Appendix Graph 1.

Table 6. Possible delays for the Upper PLD.

DEC	HEX	BIN	DELAY(U)	DEC	HEX	BIN	DELAY(U)
0	00	000000	188.8	32	20	100000	344.4
1	01	000001	196.8	33	21	100001	347.2
2	02	000010	204.8	34	22	100010	355.2
3	03	000011	207.6	35	23	100011	358
4	04	000100	212.8	36	24	100100	363.2
5	05	000101	215.6	37	25	100101	366
6	06	000110	223.6	38	26	100110	374
7	07	000111	226.4	39	27	100111	376.8
8	08	001000	231.6	40	28	101000	382
9	09	001001	234.4	41	29	101001	384.8
10	0A	001010	242.4	42	2A	101010	392.8
11	0B	001011	245.2	43	2B	101011	395.6
12	0C	001100	250.4	44	2C	101100	400.8
13	0D	001101	253.2	45	2D	101101	403.6
14	0E	001110	261.2	46	2E	101110	411.6
15	0F	001111	264	47	2F	101111	414.4
16	10	010000	269.2	48	30	110000	419.6
17	11	010001	272	49	31	110001	422.4
18	12	010010	280	50	32	110010	430.4
19	13	010011	282.8	51	33	110011	433.2
20	14	010100	288	52	34	110100	438.4
21	15	010101	290.8	53	35	110101	441.2
22	16	010110	298.8	54	36	110110	449.2
23	17	010111	301.6	55	37	110111	452
24	18	011000	306.8	56	38	111000	457.2
25	19	011001	309.6	57	39	111001	460
26	1A	011010	317.6	58	3A	111010	468
27	1B	011011	320.4	59	3B	111011	470.8
28	1C	011100	325.6	60	3C	111100	476
29	1D	011101	328.4	61	3D	111101	478.8
30	1E	011110	336.4	62	3E	111110	486.8
31	1F	011111	339.2	63	3F	111111	494.8

Table 7. Possible for the Lower PLD.

DEC	HEX	BIN	DELAY(L)	DEC	HEX	BIN	DELAY(L)
0	00	000000	414.4	32	20	100000	564.8
1	01	000001	422.4	33	21	100001	572.8
2	02	000010	430.4	34	22	100010	580.8
3	03	000011	438.4	35	23	100011	588.8
4	04	000100	433.2	36	24	100100	583.6
5	05	000101	441.2	37	25	100101	591.6
6	06	000110	449.2	38	26	100110	599.6
7	07	000111	457.2	39	27	100111	607.6
8	08	001000	452	40	28	101000	602.4
9	09	001001	460	41	29	101001	610.4
10	0A	001010	468	42	2A	101010	618.4
11	0B	001011	476	43	2B	101011	626.4
12	0C	001100	470.8	44	2C	101100	621.2
13	0D	001101	478.8	45	2D	101101	629.2
14	0E	001110	486.8	46	2E	101110	637.2
15	0F	001111	494.8	47	2F	101111	645.2
16	10	010000	489.6	48	30	110000	640
17	11	010001	497.6	49	31	110001	648
18	12	010010	505.6	50	32	110010	656
19	13	010011	513.6	51	33	110011	664
20	14	010100	508.4	52	34	110100	658.8
21	15	010101	516.4	53	35	110101	666.8
22	16	010110	524.4	54	36	110110	674.8
23	17	010111	532.4	55	37	110111	682.8
24	18	011000	527.2	56	38	111000	677.6
25	19	011001	535.2	57	39	111001	685.6
26	1A	011010	543.2	58	3A	111010	693.6
27	1B	011011	551.2	59	3B	111011	701.6
28	1C	011100	546	60	3C	111100	696.4
29	1D	011101	554	61	3D	111101	704.4
30	1E	011110	562	62	3E	111110	712.4
31	1F	011111	570	63	3F	111111	720.4

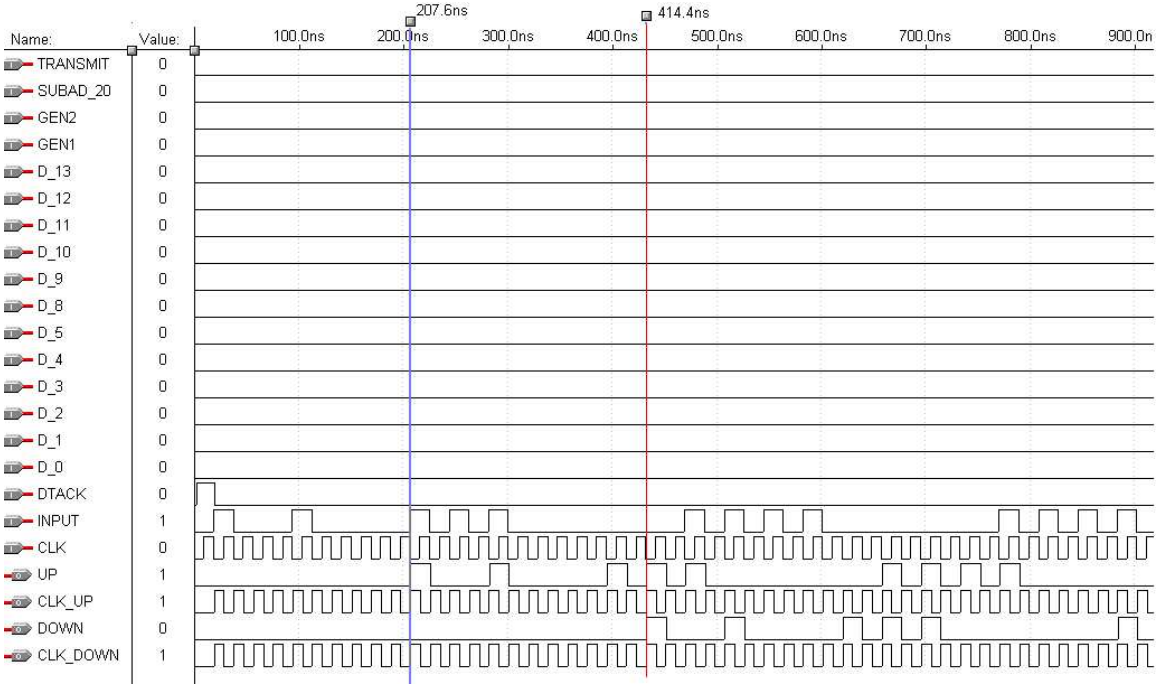

Figure 22 . Timing diagram for the minimum delay for Upper and Lower PLD

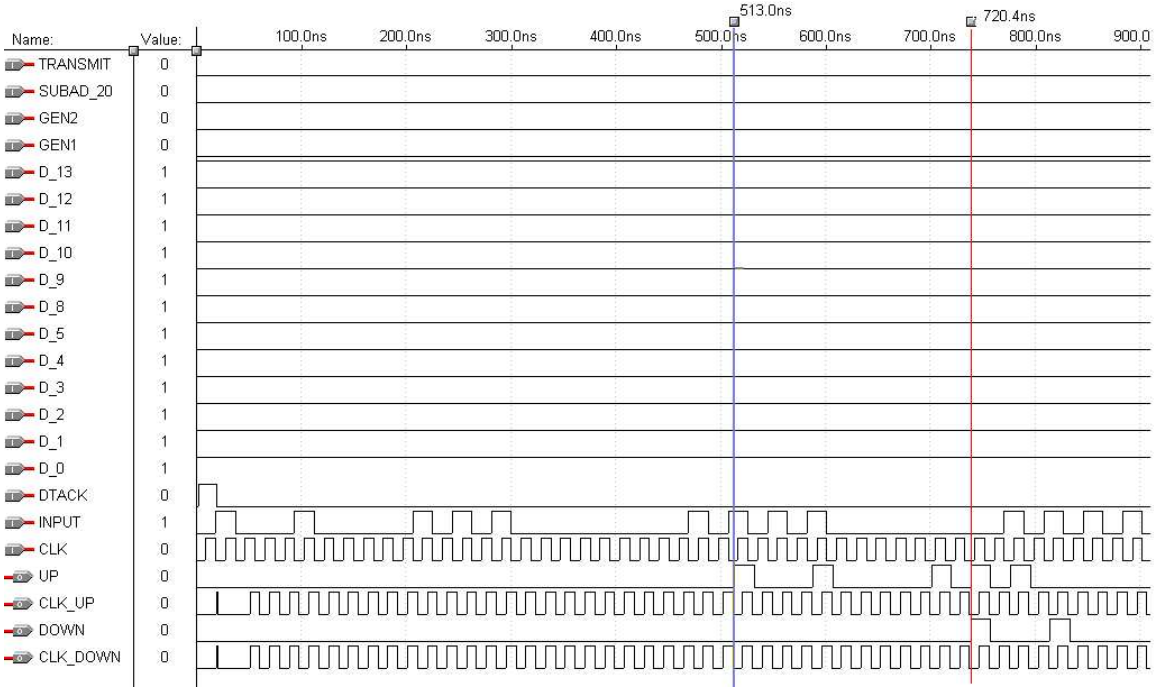

Figure 23 . Timing diagram for the maximum delay for Upper and Lower PLD

Design Note.

The MIL-STD 1553 provides a 16 bit word to program the communication block but in this version only a 12 bits are needed. To make programming the delays easier the

first 8 bits from the 16 bit data bus will be utilized with the last bits of the 8 bits as don't cares, i.e. they would not be connected to the NEW PLD. The remain 6 bits provides the required data word for the delay of the Upper PLD. The next 8 bits are treated the same, with the last two bit acting as don't cares and the remaining 6 bits provides the required data word for the delay of the Lower PLD. Table 7 gives a pictorial representation.

Table 7. Usage of the 16 bit data bus

First 8 bits								**Last 8 bits**							
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
6 bits						**X**	**X**	**6 bits**						**X**	**X**
For Upper PLD						**NC**	**NC**	**For Lower PLD**						**NC**	**NC**

In the Appendix Table 8 gives the summary of the Resource usage as produced by Altera.

6. Conclusion

The FPD group is interested in studying hard diffractions. In order for the FPD group to carry out their diffractive studies, they have to know the types particles created after each collision and the scattering angle of the proton. Obtaining the information about what types of particles is created, is given by the sub-detectors of the DØ detector. To measure the scattering angle, which is approximately 1 mrad, the FPD detector is placed far from the DØ detector. For the FPD data to be integrated into the DØ system, the FPD detector must be looking at the same event as those within the DØ detector. The positioning of the FPD detector causes need of delays in the data acquisition of the FPD so that study of the same events as those within the detector are possible. It has been calculated that there are 3 different delays.

The Sequencer delay method, described in this report can only provide two different delays. At the time of this report, it was proposed that the smallest and the middle delay would be provided by the Sequencer delay method, described in this report. The largest delay, since it approximately 60ns longer than the middle delay, that the third delay would be created form the middle delay by adjusting the integration window of the SIFT chip.

At the time of this report the New PLD, version 1, was installed on the Sequencer and primary test was done to test the validity of the design. Initial testing of the design showed that the insertion of the device was non-destructive to the normal operation of the Sequencer and that it is a valid method. However, the NRZ prime signal also has to be delayed. Adding the delays of the NRZ prime is a simple modification of Version 1. It involves adding another NRZ delay block in parallel to the existing NRZ block in Version 1.

7. References

[1] M.Utes, "Sequencer Controller", http://d0server1.fnal.gov/users/utes/webpage/seqcon.htm

[2] M. Utes, "SVX Sequencer Board", http://d0server1.fnal.gov/users/utes/webpage/svx_sequencer.htm

[3] M. Vaz , "AFE boards for FPD", http://d0br1.lafex.cbpf.br/~mario/FPD/fpdafe.html

[4] J. Anderson, "D-Zero Fiber Tracker 8 MCM Analog Front End board" http://d0br1.lafex.cbpf.br/~mario/FPD/fpdafe/JA_8mcmspec.pdf

[5] Altera, Reference book, 1996

8. Acknowledgement

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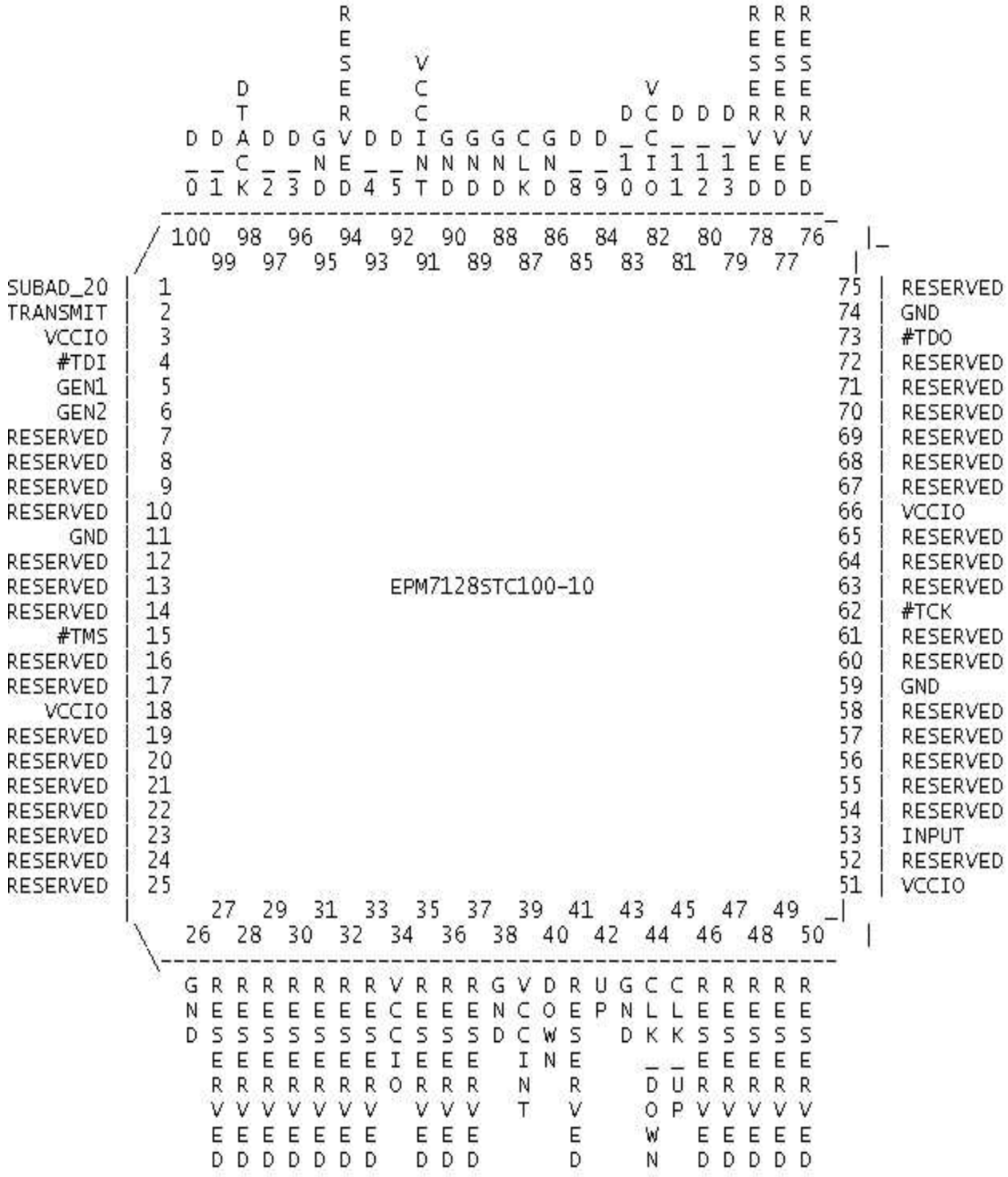
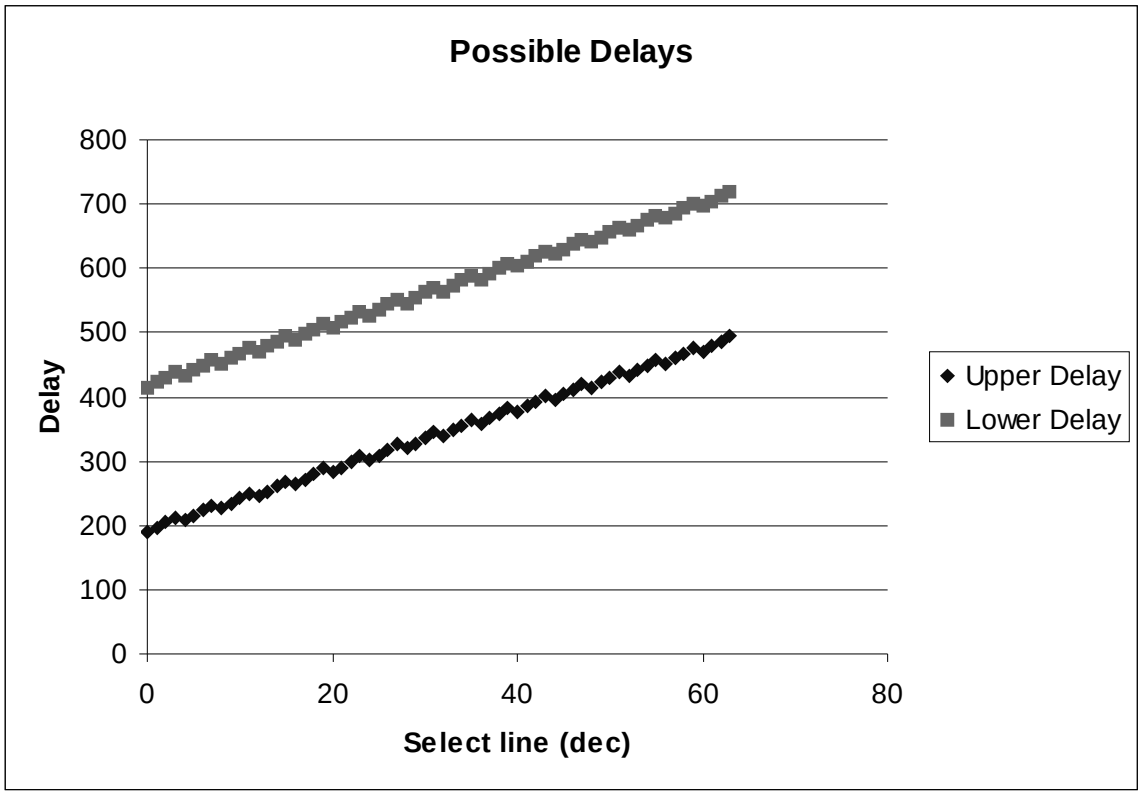
10. Appendix

Pin layout of the Version 1.


EPM7128STC100-10
1 SUBAD_20
2 TRANSMIT
3 VCCIO
4 #TDI
5 GEN1
6 GEN2
7 RESERVED
8 RESERVED
9 RESERVED
10 RESERVED
11 GND
12 RESERVED
13 RESERVED
14 RESERVED
15 #TMS
16 RESERVED
17 RESERVED
18 VCCIO
19 RESERVED
20 RESERVED
21 RESERVED
22 RESERVED
23 RESERVED
24 RESERVED
25 RESERVED
26 GND
27 RESERVED
28 RESERVED
29 RESERVED
30 RESERVED
31 RESERVED
32 RESERVED
33 RESERVED
34 VCCINT
35 RESERVED
36 RESERVED
37 RESERVED
38 GCLK1
39 VCCIO
40 RESERVED
41 RESERVED
42 GCLK2
43 GCLRN
44 RESERVED
45 RESERVED
46 RESERVED
47 RESERVED
48 RESERVED
49 RESERVED
50 TCK
51 VCCIO
52 RESERVED
53 INPUT
54 RESERVED
55 RESERVED
56 RESERVED
57 RESERVED
58 RESERVED
59 GND
60 RESERVED
61 RESERVED
62 #TCK
63 RESERVED
64 RESERVED
65 RESERVED
66 VCCIO
67 RESERVED
68 RESERVED
69 RESERVED
70 RESERVED
71 RESERVED
72 RESERVED
73 #TDO
74 GND
75 RESERVED
76 RESERVED
77 RESERVED
78 RESERVED
79 RESERVED
80 RESERVED
81 VCCINT
82 RESERVED
83 RESERVED
84 RESERVED
85 RESERVED
86 GCLK3
87 VCCINT
88 RESERVED
89 RESERVED
90 RESERVED
91 RESERVED
92 VCCINT
93 RESERVED
94 RESERVED
95 GND
96 RESERVED
97 #TDO
98 #TCK
99 RESERVED
100 DATA0



Graph1. Possible Delays for New PLD (version 1)

Table 8. Summary of Resource usage

Logic Array Block	Logic Cells	I/O Pins	Shareable Expanders	External Interconnect
A: LC1 - LC16	6/16(37%)	9/10(90%)	0/16(0%)	9/36(25%)
B: LC17 - LC32	0/16(0%)	3/10(30%)	0/16(0%)	0/36(0%)
C: LC33 - LC48	0/16(0%)	1/10(10%)	0/16(0%)	0/36(0%)
D: LC49 - LC64	3/16(18%)	0/10(0%)	0/16(0%)	3/36(8%)
E: LC65 - LC80	16/16(100%)	4/10(30%)	0/16(0%)	21/36(58%)
F: LC81 - LC96	16/16(100%)	2/10(20%)	2/16(12%)	19/36(52%)
G: LC97 - LC112	16/16(100%)	1/10(10%)	3/16(18%)	29/36(80%)
H: LC113 - LC128	16/16(100%)	6/10(60%)	1/16(6%)	22/36(61%)

Total dedicated input pins used:	1/4	(25%)
Total I/O pins used:	26/80	(32%)
Total logic cells used:	73/128	(57%)
Total shareable expanders used:	0/128	(0%)
Total Turbo logic cells used:	73/128	(57%)
Total shareable expanders not available (n/a):	6/128	(4%)
Average fan-in:	3.61	

Total fan-in: 264

Total input pins required: 7
Total fast input logic cells required: 1
Total output pins required: 4
Total bidirectional pins required: 12
Total reserved pins required 4
Total logic cells required: 73
Total flipflops required: 48
Total product terms required: 133
Total logic cells lending parallel expanders: 0
Total shareable expanders in database: 0

Synthesized logic cells: 9/ 128 (7%)

fmax = 100MHz.